Structural and Electrical Properties Dependence on annealing temperature of a-Ge:Sb/c-Si Heterojunction

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Abstract

In this work, we are Study the effect of annealing temperature on the structure of a-Ge films doped with Sb and the electrical properties of a-Ge:Sb/c-Si heterojunction fabricated by deposition of a-Ge:Sb film on c-Si by using thermal evaporation. Electrical properties of a-Ge:Sb/c-Si heterojunction include I-V characteristics in dark at different annealing temperatures and C-V characteristics and with the C-V characteristics suggest that the fabricated heterojunction was abrupt type, built in potential determined by extrapolation from $1/C^2$-V curve and show that the built - inpotential (V_{bi}) for the Ge:Sb/Si system increases with the increase of annealing temperatures.

Introduction

IV-VI semiconductors are commonly considered to be promising materials for optoelectronic, thermoelectric[1], and other IV-VI layers (chalcogenides) on Si substrates applications in the (inexpensive, stable material, high efficiency photovoltaic solar cell, bipolar, transistors, photo sensors, integrated circuit, infrared detectors, infrared light emitting diodes and electro photographic)[2,3,4,5].

There has been a rapidly growing interest in the physical properties of amorphous semiconductors such as Si, Ge. One reason for this is the extensive background knowledge and understanding of the crystalline material. The other reason is that being elemental; they lack compositional disorder [6].

The preliminary results of structural and electrical properties of this alloy film have been presented.

Experimental Work

Substrates of p-type single crystal Si wafers of resistivity (3-5) ohm-cm and orientation(111) was used in the present study. After the division of these wafers into small pieces (typically 0.8cm x 0.6cm in size), Si wafer was immersed and stirred in a chemical solution consists of 3ml HNO_3 1ml H_2O for (1 - 3) minutes. were cleaned ultrasonically by dipping in distilled water, acetone and isopropyl alcohol alternately. After cleaning, the samples were oxidized in dry oxygen [7]. The films of a-Ge:Sb were prepared by thermal evaporation in vacuum of the order of 10^{-5} torr, the rate of evaporation was equal to 9.43A/sec, onto clean silicon mirror-like side substrates at room temperature (~300K). The average thicknesses of the deposits were determined by microbalance method. The maximum error in the determination of thickness was of the order of 10% estimated for the thinnest films (Ge:Sb/Si films of thickness equals to 0.5 μm).Ohmic contacts of the electrical

properties of Ge:Sb/Si heterojunction, aluminum [8] were evaporated on the silicon side and Ge:Sb /Si side.

Theoretical Part

Heterojunction is contacts, with interesting electrical or electro- optical properties, between two different materials .They will therefore be the sites, in general, of discontinuities in all the significant semiconductor parameters: energy gap , work function , lattice parameter , and effective mass[9].

The expression for the junction capacitance per unit area of an abrupt anisotype heterojunction can be written as [10].

$$\frac{C}{A}=\left[\frac{q\varepsilon_n\varepsilon_p N_n N_p}{2(\varepsilon_n N_n+\varepsilon_p N_p)}\right]^{1/2}(V_D-V_a)^{-1/2} \quad \text{.....(1)}$$

Where N_n and N_p are the donor and acceptor concentrations respectively, ε_n and ε_p are the dielectric constant of n and p-type semiconductor respectively, V_D is the built-in junction potential, V is the applied voltage, and A is the area of the junction.

From plots of the relation between the forward current and bias voltage, the ideality factor (β) can be determined by the relation [11]:

$$\beta=\frac{q}{K_B T}\cdot\frac{V}{Ln\left(I_F/I_S\right)} \quad \text{.....(2)}$$

Where V is the forward bias voltage, I_f is the forward bias current, k_B is the Boltzmann's constant, T is the absolute temperature, q is charge of electron and I_S saturation current. From current-voltage measurements we can determine the potential barrier height (Φ_b) which can be determined by the relation:

$$J_s = A^* T^2 \exp(-q\Phi_b/K_B T) \quad \text{.....(3)}$$

Where A* is the effective Richardson constant.

Result and Discussion

XRD analysis

X- ray diffraction (XRD) studies have been carried out to identify the Ge phase present in the film. Fig.1 shows that XRD pattern recorded on Ge film, coated on slide glass substrate. The structural of film is amorphous.

I-V characteristics under dark

One of the important parameters of a heterojunction measurement is the current-voltage characteristic which explains the behavior of the resultant current with the applied forward and reverse bias voltage. Fig. (2) shows that I-V characteristic for a-Ge:Sb/c-Si heterojunction at forward and reverse bias voltage at R.T and different annealing temperatures (373,423.473)K. This result is in agreement with Chik et al[12] when thickness of films equals to 0.5 μm.

We observed that the current increases slightly with the increase of annealing temperatures because the increases of temperatures cause a rearrangement of the interface atoms and reducethe dangling bond, surface states and dislocation at interface layer between a-Ge:Sb and c-Si which leads to the improvement of the junction characteristics .

Also, we can notice from table (1) that the value of the ideality factor and potential barrier height increases but saturation current decreases with the increase of annealing temperature. This behavior attributed to the improvement of crystal structure at interface layer ,also the reduction of dangling bonds as well as the density of states in a-Ge:Sb.

C-V characteristics

The junction capacitance variations as a function of the reverse bias (0 – 1.2) volt at frequency equal to 100KHz has been studied, for a-Ge:Sb/c-Si heterojunction at different thicknesses of Ge:Sb layer and annealing temperatures are showed in Fig. (3). It is clear that the capacitance decreases with the increase of the reverse bias voltage and annealing temperature. This result is confirmed by equation (1) and the decreae was non-linear as shown in Fig. (3).

We can observe from Table (2), that the capacitance at zero bias voltage (C_o) decreases with the increasing of the annealing temperatures for a-Ge:Sb/c-Si junctions and this behavior is due to the surface states which leads to an increase in the depletion layer and a decrease of the capacitance.

The inverse capacitance square is plotted against applied reverse bias voltage for a-Ge:Sb/c-Si heterojunction at different annealing temperatures as shown in Fig. (4).

The plots revealed straight line relationship which means that the junction was of an abrupt type. The interception of the straight line with the voltage axis at ($1/C^2 = 0$), represents the built-in potential.

We can see from table (2) and that the variation of built-in potential (V_{bi}) from 0.589 to 0.893 Volt when annealing temperatures changes from room temperature to 473 K.

Conclusion

We get from the study the effect of annealing temperature on the structure of Ge:Sb and electrical properties of n-Ge:Sb/p-Si heterojunction the junction is abrupt type and the built - in potential (Vb_i.) for the n-Ge:Sb/p-Si System was found to increase with the increase of annealing temperature.

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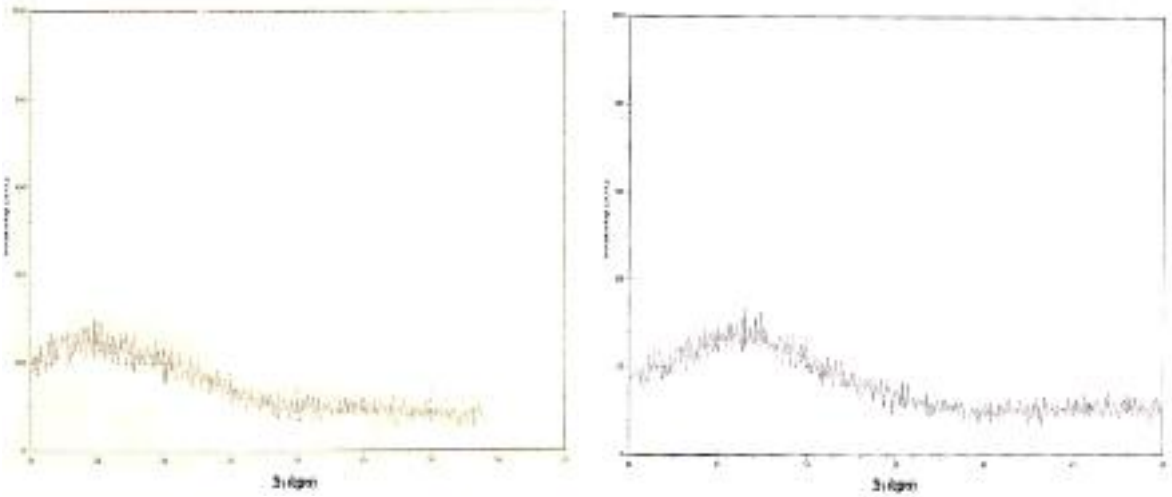
Table (1): values of ideality factor (β), saturation current (Is) and potential barrier height (Φ_b) for a-Ge:Sb/c-Si heterojunction with different thicknesses and annealing temperatures.

T_a (K)	β	I_s (μA)	Φ_b(eV)
R.T	1.591	0.0104	0.344
373	1.621	0.0096	0.345
423	1.627	0.0085	0.347
473	1.695	0.0067	0.352

Table (2): values of C_o and V_{bi} for a-Ge:Sb/c-Si heterojunction with different thicknesses and annealing temperatures.

T_a (K)	C_o (pF)	V_{bi} (Volt)
R.T	18.1	0.589
373	16.11	0.667
423	11.88	0.727
473	10.19	0.893



(a) (b)

Fig.(1): X-ray diffraction of a-Ge films at (a) T_a =R.T (b) T_a =473K

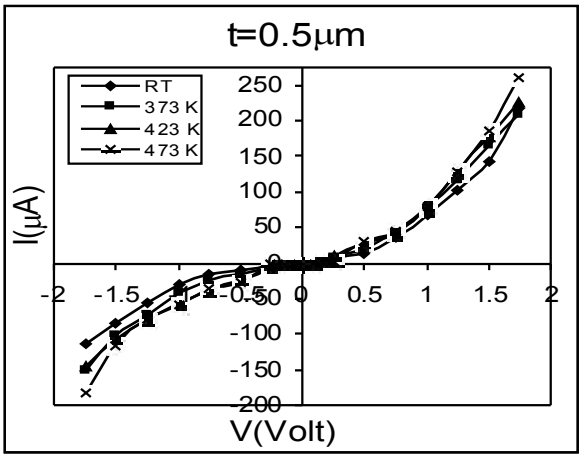


Fig. (2): I-V characteristics in the dark for a-Ge:Sb/c-Si heterojunction at forward and reverse bias voltage at different annealing temperatures

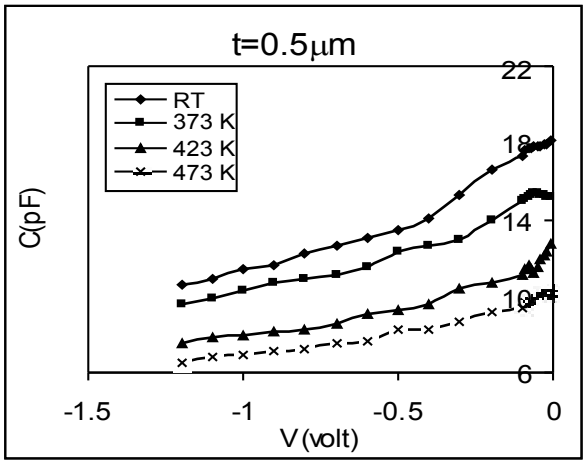


Fig. (3): The variation of capacitance versus reverses bias voltage for a-Ge:Sb/c-Si heterojunction for different annealing temperatures

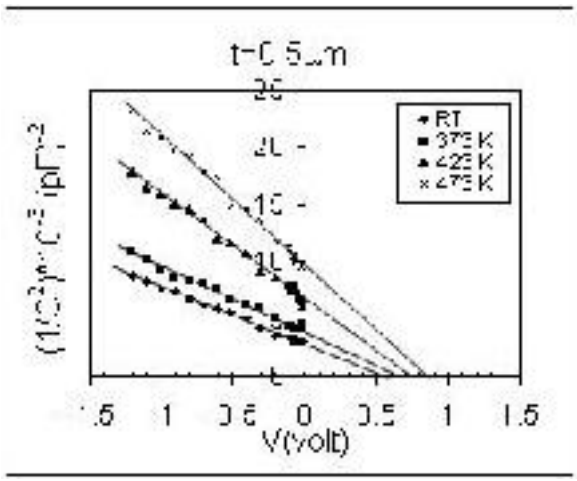


Fig.(4): The variation of $1/C^2$ versus reverses bias voltage for a-Ge:Sb/c- Si heterojunction at different annealing temperatures

اعتماد الخواص التركيبية والكهربائية على التلدين للمفرق الهجيني a-Ge:Sb/c-Si

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الخلاصة

في هذا البحث دراس تأثير التلدين في الخواص التركيبية لاغشية a-Ge المطعمة بـ Sb والخواص الكهربائية للمفرق ألهجيني a-Ge:Sb/c-Si الناتج من ترسيب a-Ge:Sb بطريقة التبخير الحراري على السليكون. الخواص الكهربائية للمفرق الهجيني تتضمن خصائص التيار-فولتية في حالة الظلام وبدرجات تلدين مختلفة وخصائص سعة-فولتية . ومن خصائص سعة-فولتية تبين ان المفرق الهجيني كان من النوع المنحدر وان جهد البناء تم تحديده من منحني الفولتية ومقلوب مربع السعة وتبين ان جهد البناء للمفرق الهجيني يزداد بزيادة درجات حرارة التلدين.